FIG. 1

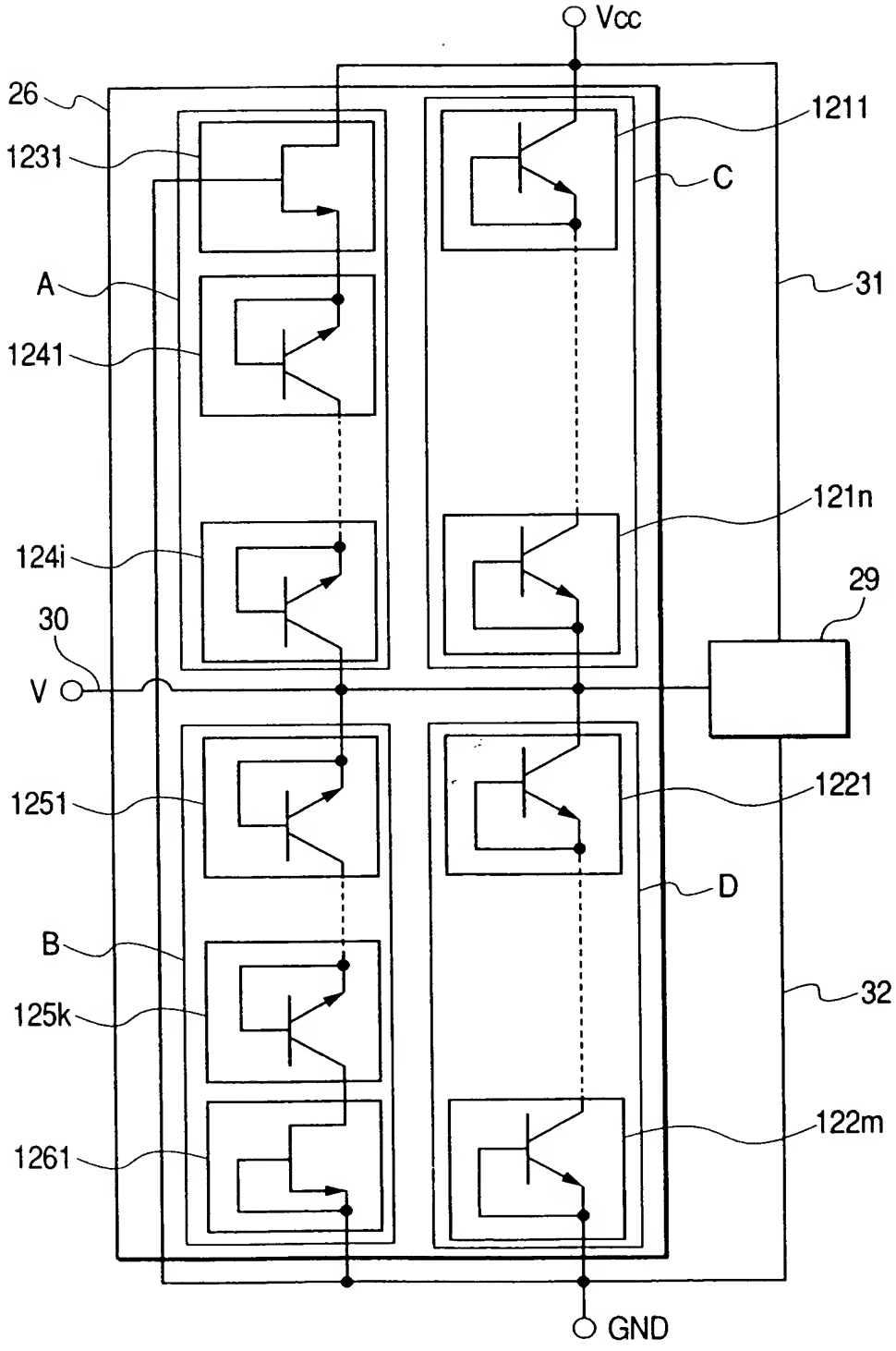
Vcc
26
1231
1211
C
A
31
1241
121n
124i
29
30
V
1251
1221
D
B
32
125k
122m
1261
GND

FIG. 2(A)

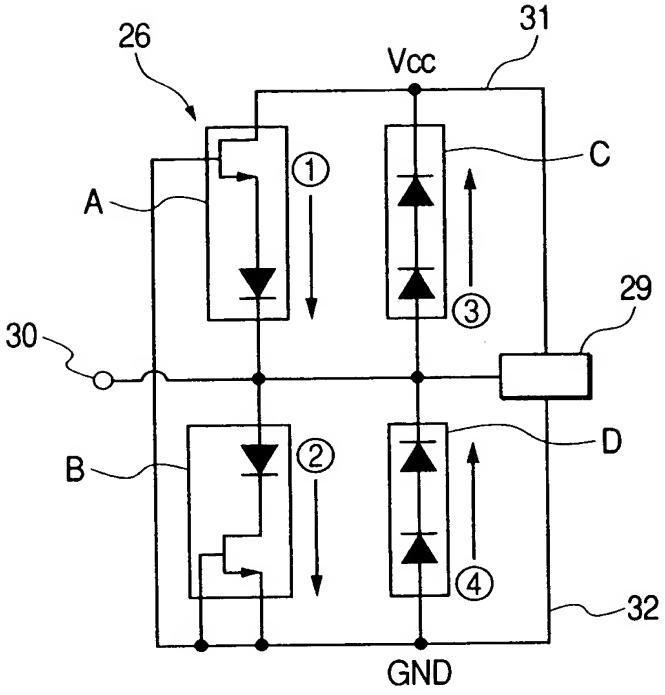

FIG. 2(B)

No.	NOTED PIN & POTENTIAL DIFFERENCE	CURRENT PATH
1	Vcc(+), GND(−)	①→②
2	Vcc(+), S(−)	①
3	S(+), GND(−)	②
4	Vcc(−), S(+)	③
5	Vcc(−), GND(+)	④→③
6	S(−), GND(+)	④

FIG. 3

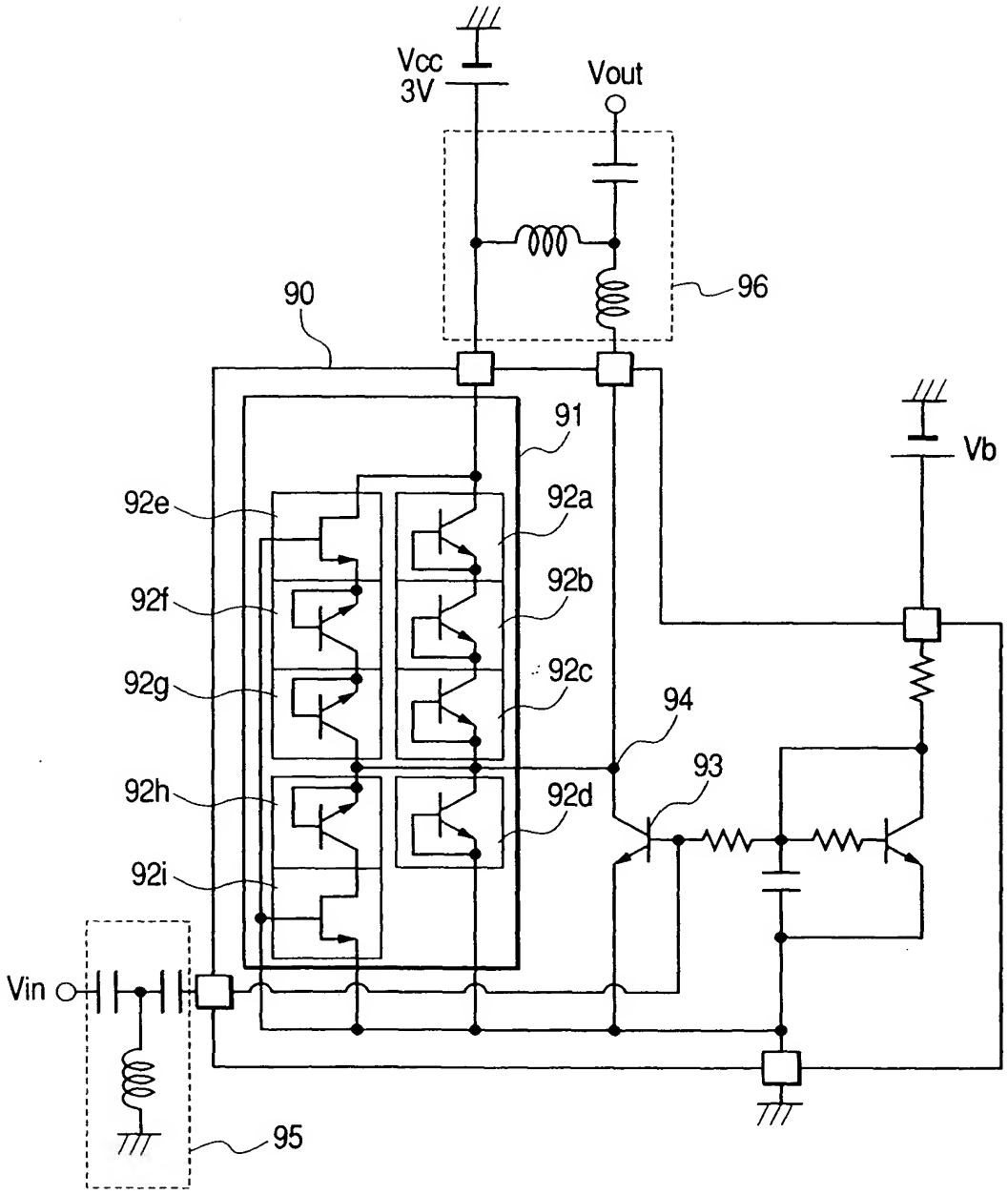
Vcc
3V
Vout
96
90
91
Vb
92e
92a
92f
92b
92g
92c
94
93
92h
92d
92i
Vin
95

FIG. 4

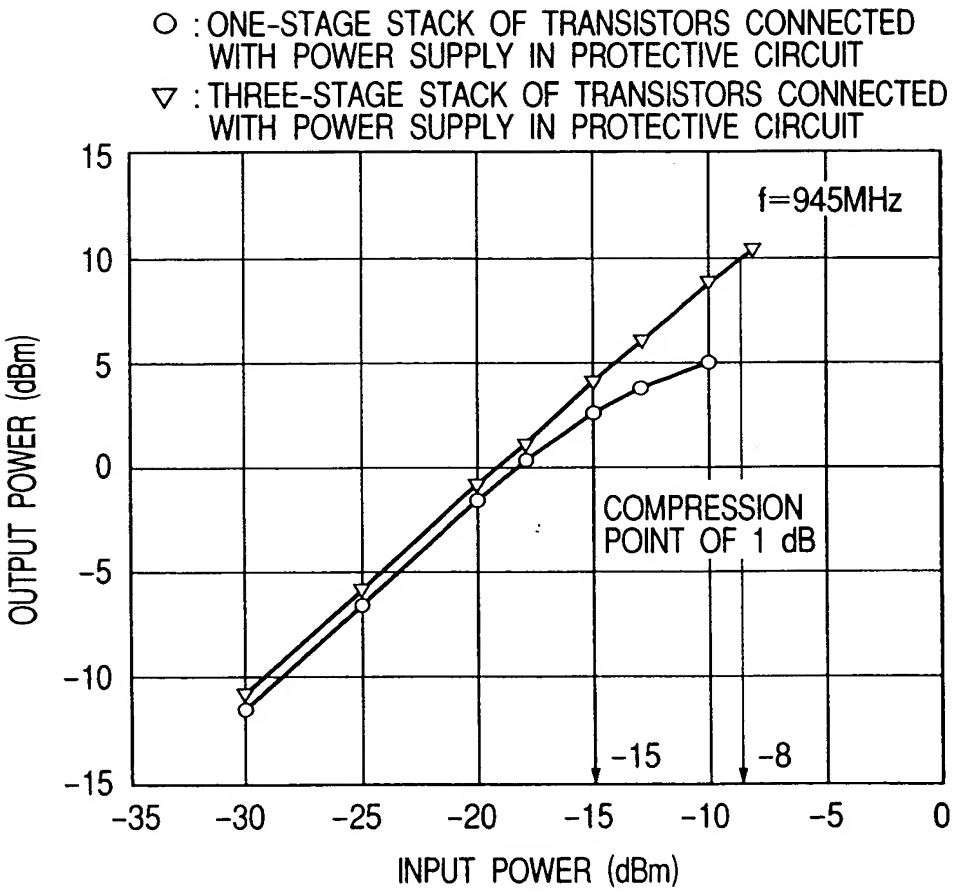
○ : ONE-STAGE STACK OF TRANSISTORS CONNECTED WITH POWER SUPPLY IN PROTECTIVE CIRCUIT
▽ : THREE-STAGE STACK OF TRANSISTORS CONNECTED WITH POWER SUPPLY IN PROTECTIVE CIRCUIT
f=945MHz
COMPRESSION POINT OF 1 dB
-15
-8
OUTPUT POWER (dBm)
INPUT POWER (dBm)
15
10
5
0
-5
-10
-15
-35
-30
-25
-20
-15
-10
-5
0

FIG. 5

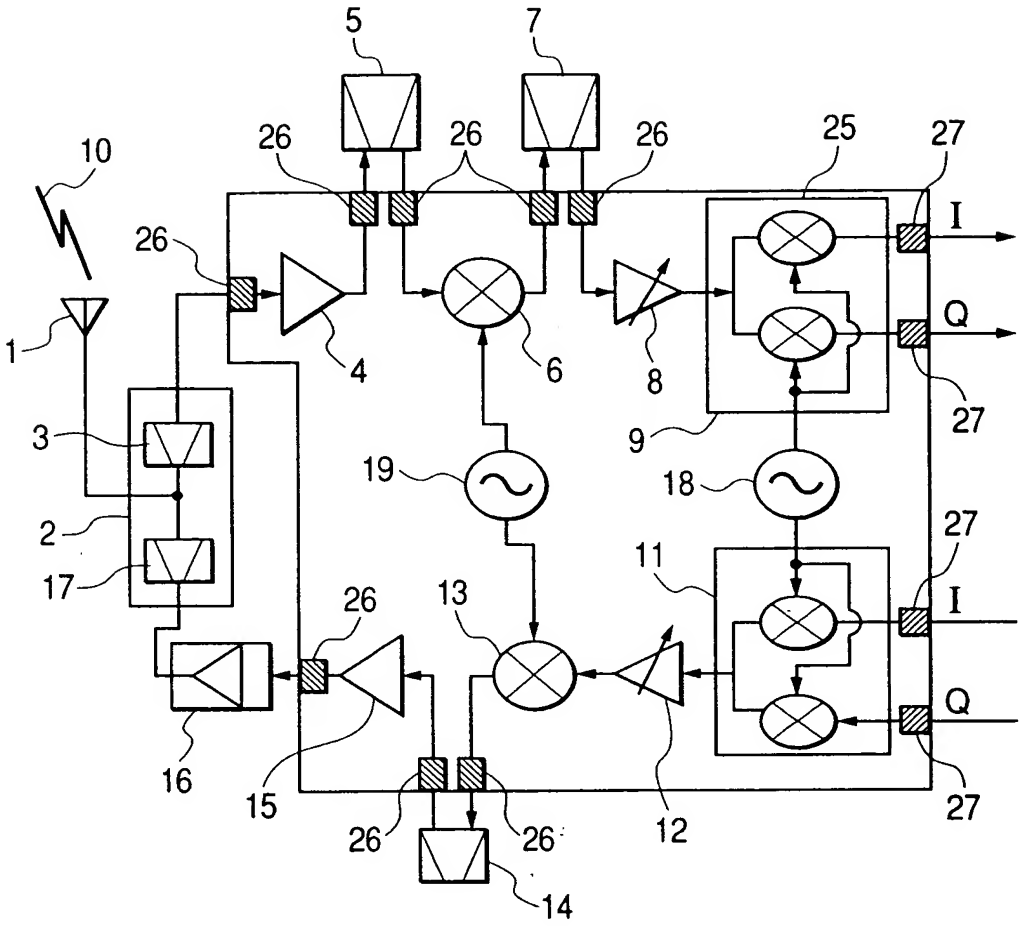
5
7
10
26
26
26
25
27
26
I
Q
1
4
6
8
27
3
9
19
18
2
17
11
27
26
13
I
Q
16
15
12
27
26
26
14

FIG. 6

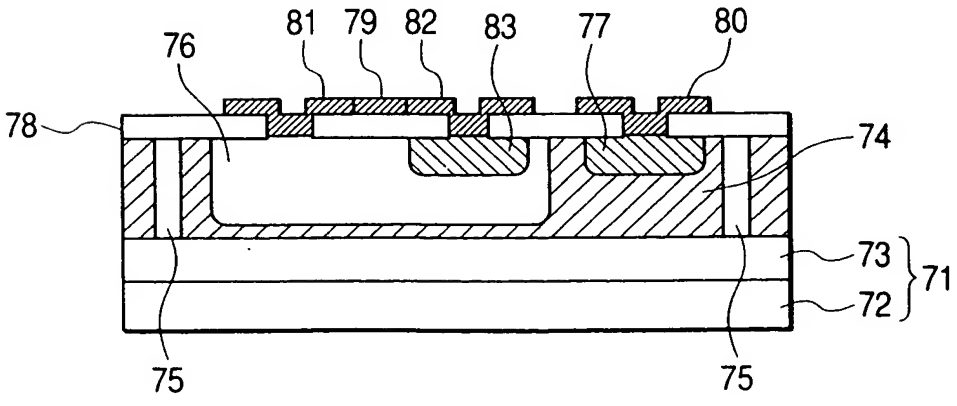
81
79
82
83
77
80
76
78
74
73
71
72
75
75

FIG. 7

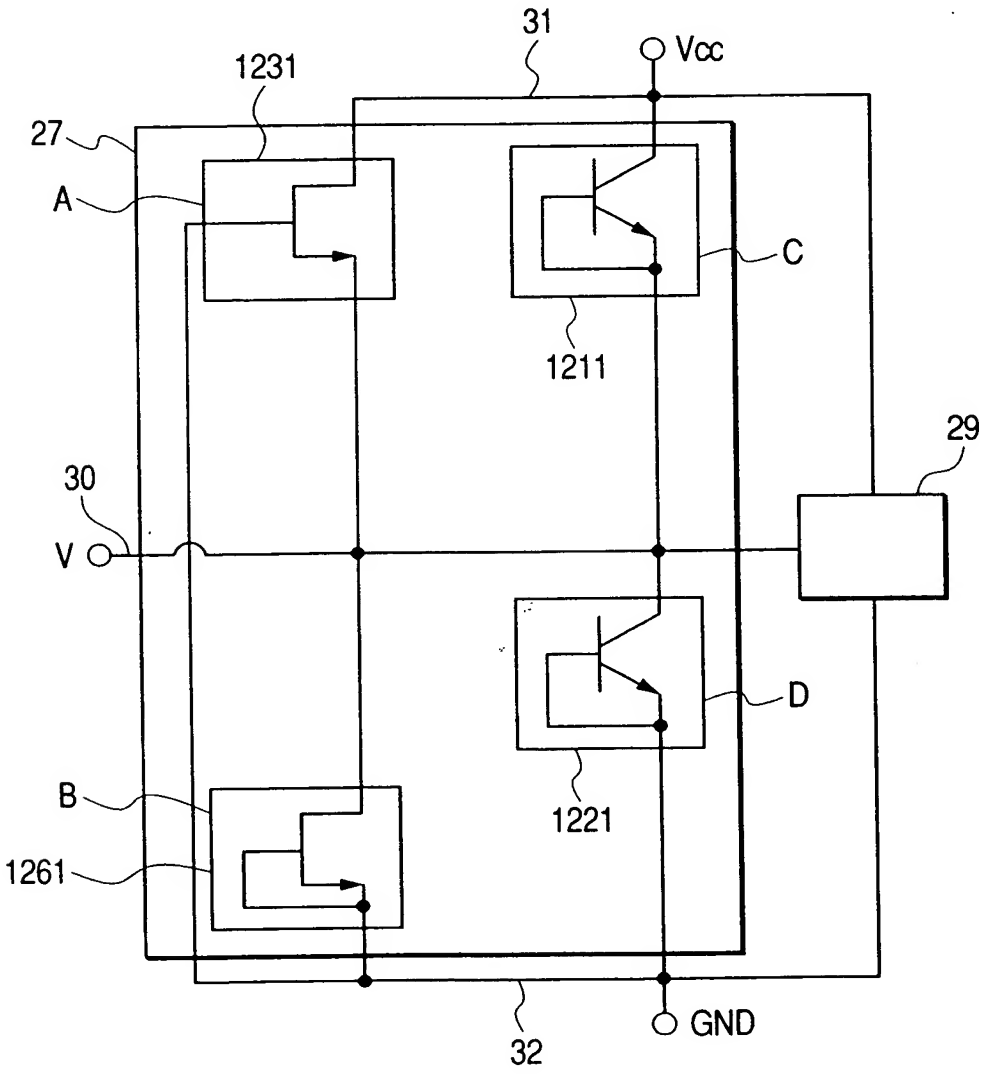

FIG. 8

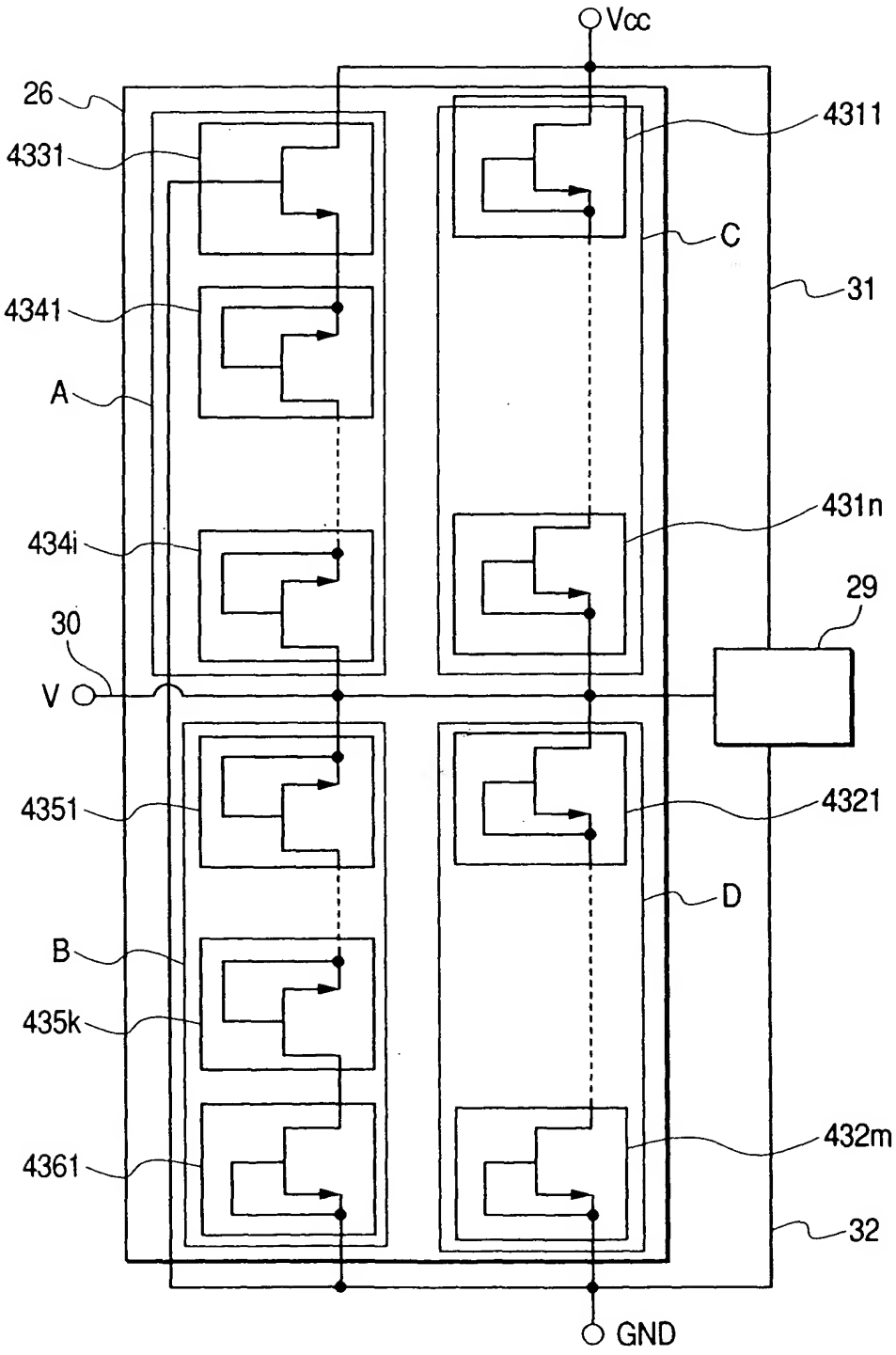
Vcc
26
4331
4311
C
31
4341
A
431n
434i
29
30
V
4351
4321
D
B
435k
4361
432m
32
GND

FIG. 9

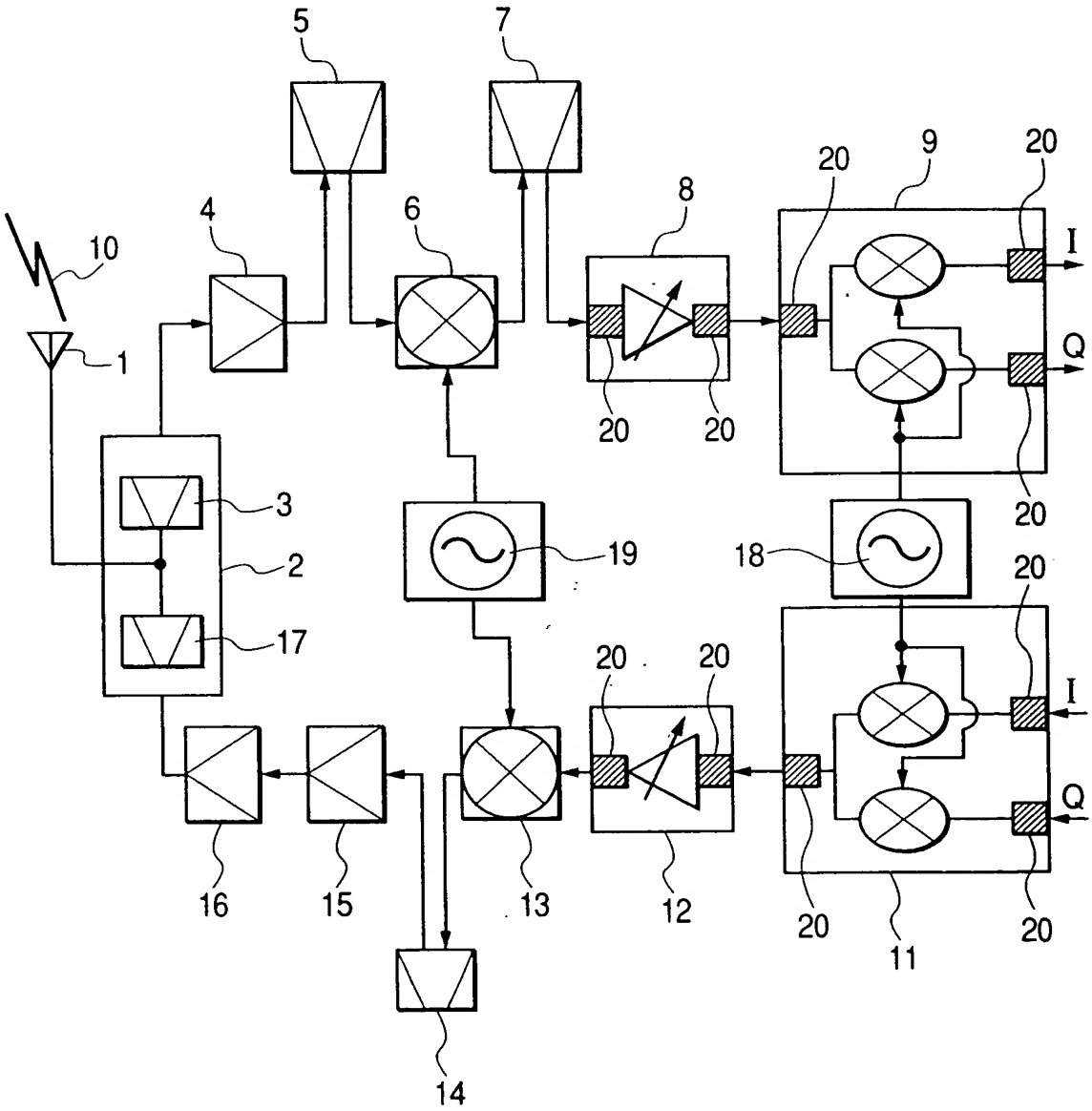
5
7
4
6
8
20
9
20
10
I
1
Q
20
20
20
3
19
18
20
2
17
20
20
I
Q
16
15
13
12
20
11
20
14

FIG. 10

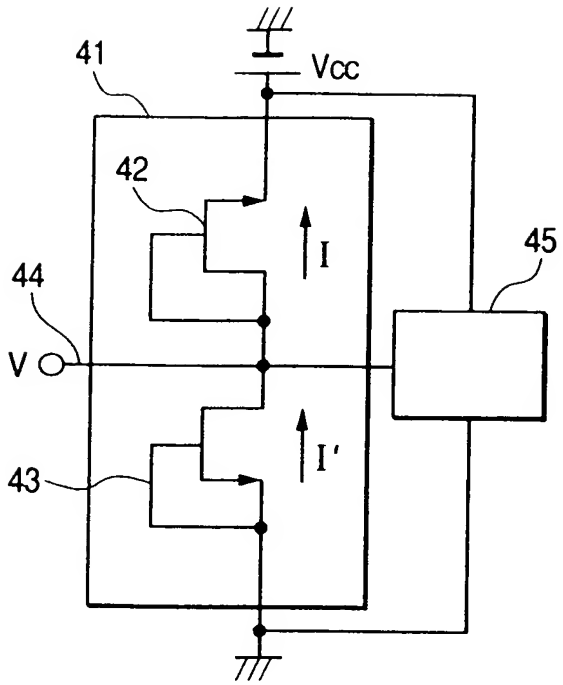

FIG. 11
PRIOR ART

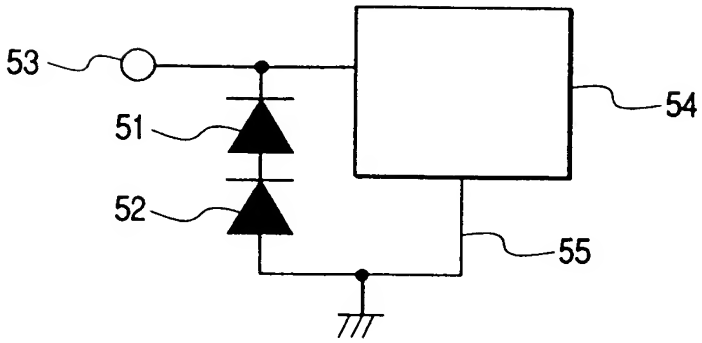

FIG. 12

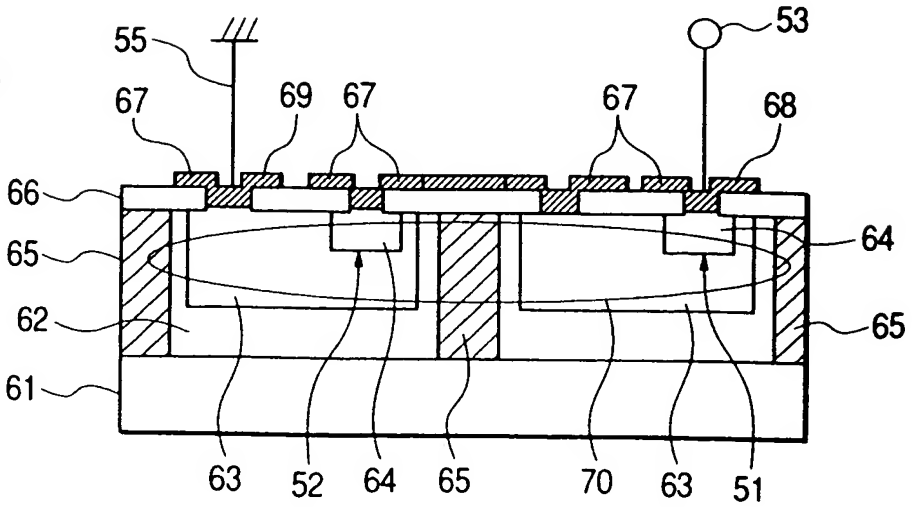

FIG. 13(A)

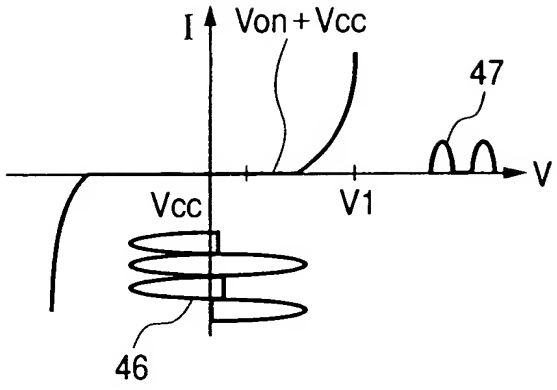

FIG. 13(B)

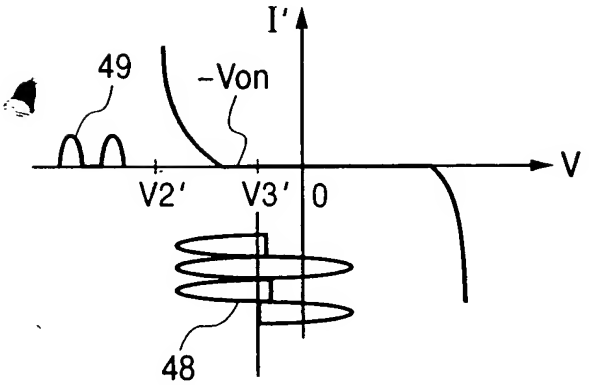

FIG. 14